

ABSTRACT OF THE DISCLOSURE

Disclosed is a digital-to-analog (D/A) converter with low skew and glitches. The D/A converter has current cells each outputting a different current amount and current switches selectively enabling the current cells, and obtains an analog signal from voltages corresponding to output currents of the current cells by operating the current switches, characterized in that the current switches are each provided with MOS transistors each having an adjusted aspect ratio so as to have a constant capacitance load regardless of the output current amounts from the current cells. In such a D/A converter, parasitic capacitances of MOS transistors provided in the current switches are adjusted constant regardless of output current amounts, so that the D/A converter can operate at a high speed with low skew and glitch.